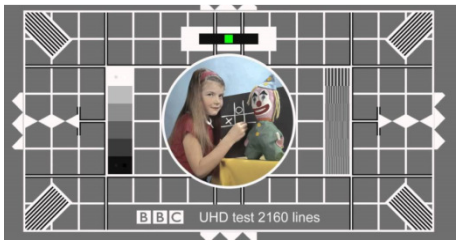
Tel: 0118 971 1930
Email: si@alspcb.com

TV at 24Gbps

by Christopher Halford
Advanced Layout Solutions Ltd
chris.halford@alspcb.com

It is over a quarter of a century since TV 'went digital'. In 1989 SMPTE (The Society of Motion Picture and Television Engineers) standardised the serial digital interface (*SDI*) as SMPTE-259M. The goal of this standard was to transport uncompressed, broadcast-quality video through legacy 75Ω coax cables and BNC connectors. Over the following years screen resolutions have grown steadily, matched by a corresponding increase in signalling data-rate. Initial high-definition standards (*HD-SDI*) in the late 1990s escalated data-rates from hundreds of megabits to nearly one and a half gigabits per second. Eight years later, SMPTE-424M (*3G-SDI*) then doubled this data-rate to almost three gigabits per second, giving us the '1080p' format that we have enjoyed for almost a decade.

The latest standards (commonly referred to as *4K* or *UHD-TV*) require 6Gbps and 12Gbps data-rates in order to deliver ultra-high-definition images at 30Hz and 60Hz respectively. Furthermore, the working group's current roadmap cites 24Gbps for future standards, whilst still using variants of basic BNC connectors and 75Ω coax cabling.

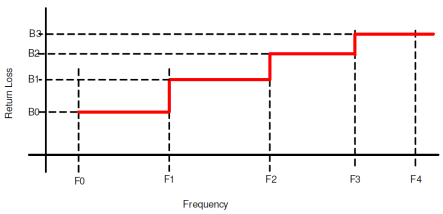


Electrical Implications

The significance of this evolution is that, in order to move TV images between pieces of equipment (albeit uncompressed broadcast-quality TV), the use of a 12Gbps data-stream is required. This stream is nearly 100x faster than the original *SDI* standard, and sees the bit period (UI) reduce from ~7ns to ~83ps. In physical terms, this means that a single bit of data that, under the original *SDI* standard, occupied 1.11m of cable or PCB trace would now occupy only 13mm. Logic level transitions, originally in the nanosecond regime, will now be only tens of picoseconds in duration. The frequency content of such a signal can present huge challenges to engineers, especially if designing to these higher data-rates is unfamiliar to them.

Hardware Design

The *HD-SDI* signal can successfully traverse extremely long runs of coaxial cable, typically up to 100m, due to the uniform transmission-line properties that a coaxial cable provides. In contrast, launching into and exiting from such a transmission-line can be very difficult if signal integrity is to be preserved. Invariably, at each end of the cable will be a mated BNC connector and a printed circuit board carrying an *SDI* Tx/Rx IC. The final few millimetres of a link usually involve a very complex structure of connector bodies, connector pins, printed circuit board traces/vias and surface mount passive components. The objective for the connector and PCB designer is to provide a path that, as closely as possible, appears to be a continuation of the75Ω transmission-line, with minimal discontinuities, all the way to the receiving device. This is not a trivial task as connectors are mechanically complex, being detachable and physically robust. The PCB is, by its very nature, a planar 2D structure and the transition from a coaxial 3D medium such as the cable and connector to a planar 2D medium will invariably create an impedance discontinuity of some degree. In order to comply with the SMPTE standards, this discontinuity must be managed and a return loss mask is published so that compliance can be established. In order to satisfy this mask, the return loss must be kept below -15dB, -10dB, -7dB and -4dB as the frequency increases from 5MHz to 12GHz.

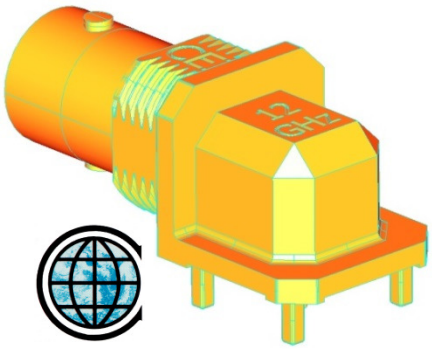


The final plateau in the mask requires that the return loss between 6GHz and 12GHz be a worst case of -4dB. Achieving this return loss is not straight forward in this frequency band and many iterations of PCB layout may be required in order to fine tune and finalise the design.

To predict whether or not the PCB layout is sufficiently optimised to meet the *4K* mask, signal integrity analysis will be required. At these data-rates the physical features of the PCB and connector are large compared to the wavelength of the signal, and in order to accurately capture the effects of the complex structures, electromagnetic solvers are required to be used on both the connector and PCB. These solvers must be 'full-wave' 3D types that provide a solution for the full Maxwell's equations without simplification.

12G-SDI Connectors

Cambridge Connectors has specialised in bespoke RF coaxial connectors for over 30 years. Their latest ranges of BNC and Micro BNC offerings are designed to support the *12G-SDI* standard, with a focus on low return loss up to and above 12GHz. Using CST Microwave Studio® the company is able to evaluate the performance of their new products throughout the design phase and provide return loss figures in Touchstone (S-Parameter) format to their customers. The return loss figures for these connectors can be as low as -24dB at 12GHz, indicating that only 0.4% of power is reflected back.



Users of the Advanced Layout Solutions OrCAD CIS Library will find the complete range of Cambridge *SDI* and *HD-SDI* BNC and Micro-BNC connectors in the OrCAD parts database. Each part is listed with its own parametric data, schematic symbols and PCB footprints.

Printed Circuit Board Simulation

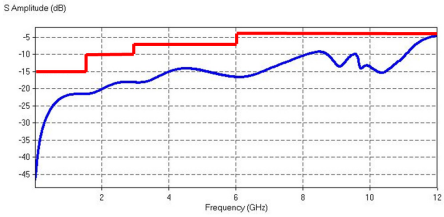
When using a high performance connector, the vast majority of the discontinuity is going to be caused by the interface between it and the PCB and from the PCB layout itself. The circuit between connector and IC is usually very simple, at most comprising a 75Ω trace and some passive components, but despite this, the structure is often complex, involving signal vias, ground plane shapes, return-current vias, etc. At these frequencies even the slightest adjustment to the structure (e.g. the ground plane clearance around a via) can have a major impact on the measured return loss.

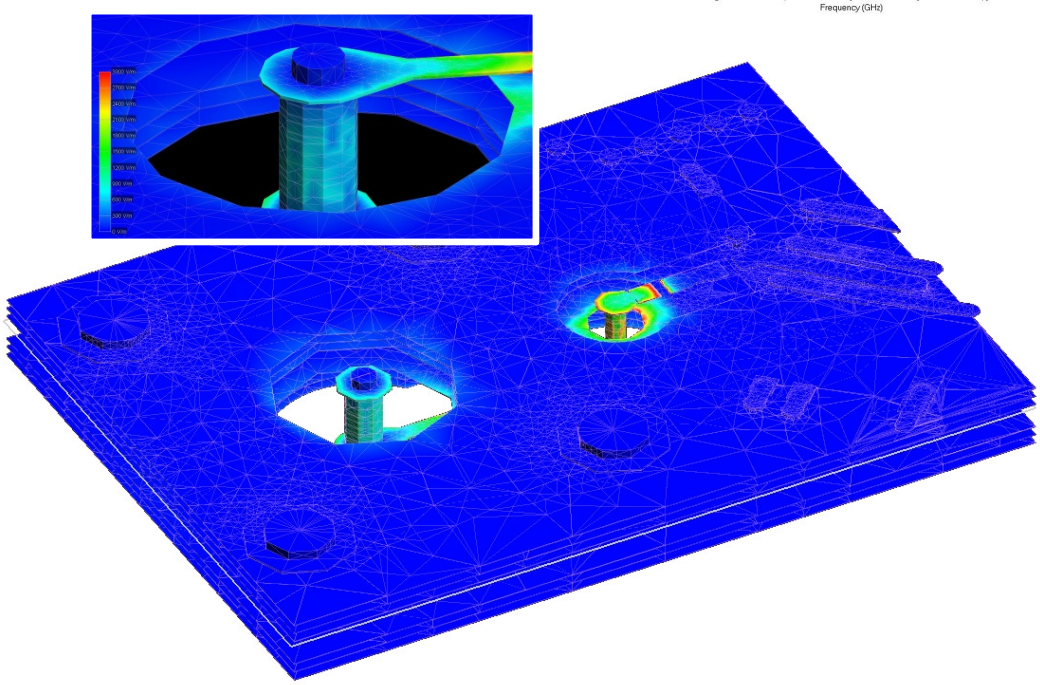
Using the Sigrity™ full-wave 3D-FEM solver from Cadence Design Systems, Advanced Layout Solutions is able to simulate the full PCB structure at the *HD-SDI* launch and receive ends of a link. The FEM approach (finite element method) breaks down a complex problem into a mesh of many smaller elements, making it an ideal tool for solving complex geometries and 3-dimensional problems. These element equations are recombined into a global system of equations to yield a final solution.

Although generally thought to be 'slow' simulations, the use of multi-processor, multi-core machines with large amounts of RAM on hand makes this methodology practical to work with.

In the case study that provided the images below, many simulation iterations were performed whilst exploring antipad sizes, via stubs, ground return vias, etc. A final layout was found that gives a satisfactory return loss of up to 12GHz for the PCB in isolation. The return loss of the connector and PCB are finally cascaded and S-Parameters are extracted for the complete system (connector to IC pin). Techniques are sometimes required to legitimise this approach, e.g. if a connector model includes a portion of PCB structure then this must first be de-embedded before a cascade is valid.

The resultant return loss (blue) is shown below against the SMPTE mask (red) from 5MHz to 12GHz.





PCB Structure Modelled in Sigrity™ 3D-FEM

For more information on PCB design & signal integrity please contact:

Advanced Layout Solutions Ltd
Fronds Park, Frouds Lane, Aldermaston,
Reading, Berkshire, RG7 4LH, UK
Tel: +44 (0) 118 971 1930
Fax: +44 (0) 118 971 1931
http://www.signalintegrityanalysis.com
mailto:si@alspcb.com

For more information on Cambridge Connectors please contact:

Cambridge Electronic Industries Ltd,
Pembroke Avenue, Waterbeach,
Cambridge, CB25 9QR, UK
Tel: +44 (0) 122 386 0041
Fax: +44 (0) 122 386 3625
http://www.cambridgeelectronics.com
mailto:info@cambridgeconnectors.com

Spring 2015